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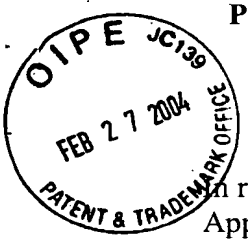

Patent

Customer No.: 31561
Docket No. 7857-US-PA
Application No.: 10/064,882

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Applicant	: Jong et al.
Application No.	: 10/064,882
Filed	: Aug. 27, 2002
For	: HEXAGONAL GATE STRUCTURE FOR RADIATION RESISTANT FLASH MEMORY CELL
Art Unit	: 2814
Examiner	: PIZARRO CRESPO, MARCOS D

TRANSMITTAL LETTER

002-1-703-305-0942

(Via fax: 16 pages, followed by confirmation copy via courier)

Assistant Commissioner for Patents
Arlington, Virginia 22202

In response to the Notice of Appeal filed on January 19, 2004, please find the relevant paper in response to it. Following the fax transmission, a hard copy via courier will also be forwarded to the Office.

Enclosed documents via courier will include:

- ☒ Appeal Brief in (14) pages
- ☒ Fax confirmation report
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Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Patent

Customer No.: 31561
Docket No. 7857-US-PA
Application No.: 10/064,882

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE JONG et al.

Application for Patent

Filed August 27, 2002

Serial No. 10/064,882

FOR:
HEXAGONAL GATE STRUCTURE FOR RADIATION RESISTANT FLASH MEMORY CELL

APPEAL BRIEF

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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real parties in interest are Fuh-Cheng Jong and Kent Kuohua Chang, the inventors named in the subject application, and MACRONIX International Co., Ltd., the assignee of record.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals and/or interferences.

III. STATUS OF THE CLAIMS

A total of 4 claims were presented during prosecution of this application. Applicant appeals rejected claims 12-15.

IV. STATUS OF THE AMENDMENTS

An amendment was filed prior to Final Rejection, on August 26, 2003, and the amendment includes cancellation of claims 1-11, addition of new claims 12-15, and changes to specification. An amendment was filed after the Final Rejection, and the amendment includes changes to claim 12 and specification, which were for clearly describing the invention and to correcting typographic errors. Appellants' reply had overcome the objection to the drawings raised in the Final Rejection (please see Advisory Action, mailed on December 17, 2003, Paper No. 6, page 2).

V. SUMMARY OF THE INVENTION

The present invention is directed to an NROM memory cell structure. The cell structure includes a source region and a drain region formed inside the substrate, and a gate structure including an oxide-nitride-oxide (ONO) layer and a control gate layer sequentially

stacked on the substrate (120a-c as the ONO layer in FIG. 2). The gate structure has a waist portion, as a hexagonal shape when viewed from the top for example, which is wider than two ends adjacent to the source region and the drain region (FIG. 1).

More specifically, the present invention provides an NROM memory cell structure comprising a gate structure having a waist portion, which is wider than the source region or the drain region, and an ONO composite layer sandwiched between the gate structure and the substrate such that, during a programming operation, a source-side electron injection is minimized. Moreover, as a portion of the gate structure close to the source region serves as an equivalent source region in a programming operation, an overall size of the equivalent source region is greater than the drain region (FIG. 3) thereby preventing second bit effect.

A copy of the claims 12-15 with elements read on but not limited to FIGs. 1-4 of the drawings involved in the appeal is presented in the appendix below.

VI. ISSUES

Were claims 12-15 properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishi et al. (US-5,760,454, hereinafter Nishi) in view of Takiyama et al. (US-5,559,351, hereinafter Takiyama)?

VII. GROUPING OF THE CLAIMS

Applicant proposes one group of claims to stand or fall together.

VIII. ARGUMENTS

A. The related law

The inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed. Hartness International, Inc. Vs. Simplimatic Engineering Co., 819 F2d 1100, 1108, 2 USPQ 2d 1826 (Fed. Cir. 1987).

It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention using the Applicant's structure as a template and selecting elements from references to fill the gaps. In re Gorman, 933 F. 2d 982, 987, 18 USPQ 2d 1885 (Fed. Cir. 1991).

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

A person of ordinary skill in the art is also presumed to be one who thinks along the line of conventional wisdom in the art and is not one who undertakes to innovate. Standard Oil Co. Vs. American Cyanamid Co., 774 F. 2d 448, 227 USPQ 293, 298 (Fed. Cir. 1985).

It should not be necessary for this court to point out that a patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. In re Sponnoble, 405 F. 2d 578, 160 USPQ 237, 243-4 (CCPA 1969).

The problem confronted by the inventor must be considered in determining whether it would have been obvious to combine references in order to solve that problem. Diversitech Corp. Vs. Century Steps, Inc., 850 F. 2d 675, 679, 7 USPQ 2d 1315 (Fed. Cir. 1988).

A prima facie case of obviousness requires that the reference teachings "appear to have suggested the claimed subject matter." In re Rinehart, 531 F.2d 1048, 189 USPQ 143, 147 (CCPA 1976).

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." In re Lalu, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

B. The rejections

Claims 12-15 were improperly rejected under 35 U.S.C. § 103(a) as being being unpatentable over Nishi et al. (US-5,760,454, hereinafter Nishi) in view of Takiyama et al. (US-5,559,351, hereinafter Takiyama).

1. The rejections

The Office Action rejectged Claims 12-15 under 35 U.S.C. § 103(a) as being being unpatentable over Nishi et al. (US-5,760,454, hereinafter Nishi) in view of Takiyama et al. (US-5,559,351, hereinafter Takiyama).

The Final Office Action, dated August 26, 2003, rejected claims 12-15 under 35 U.S.C. § 103(a) as being unpatentable over Nishi (US 5,760,454) in view of Takiyama (US 5,559,351) (Final Office Action, at pages 3-4). The Examiner states that "Nishi shows [] most aspects of the instant invention including a memory cell structure formed on a

substrate" but "fails to specify the material of the gate oxide," and that "Takiyama [] teaches that Nishi's gate oxide may be an oxide-nitride-oxide (ONO) layer." The Final Office Action held that it would have been obvious at the time of the invention to one of ordinary skill in the art "to have an oxide-nitride-oxide layer as Nishi's oxide, as taught by Takiyama, since ONO layers are commonly known in the semiconductor art for their use as gate oxides." (Final Office Action, at pages 3-4).

2. The prior art

Nishi (US-5,760,454): Nishi Patent is directed to "a MOS transistor" having a hexagon gate structure (1) formed on a substrate, and a trapezoidal source (2) and a trapezoidal drain (3) formed on both sides of the gate structure (1) (Nishi, col. 3, lines 59-63, Figure 6). Nishi teaches a structure of a gate for miniaturizing the device without reducing the operating speed of the MOS device (Nishi, Abstract; col. 1, lines 47-50).

Takiyama (US-5,559,351): Takiyama Patent is also directed to "a MOS transistor" for controlling the threshold voltage without reducing the dielectric breakdown voltage of the silicon (gate) oxide. Further, Takiyama discloses that the silicon oxide "MOS transistor" may be replaced by an ONO composite layer to function as a gate oxide layer of a "MOS transistor" (Takiyama, col. 2, lines 56-61; col. 13, lines 40-42).

The Office Action relied upon Takiyama to disclose an ONO composite layer of a MOS device.

3. The prior art distinguished

Under 35 U.S.C. § 103(a)

The Final Office Action, dated August 26, 2003, rejected claims 12-15 under 35 U.S.C. § 103(a) as being unpatentable over Nishi (US 5,760,454) in view of Takiyama (US 5,559,351) (Final Office Action, at pages 3-4). The Examiner states that "Nishi shows [] most aspects of the instant invention including a memory cell structure formed on a substrate" but "fails to specify the material of the gate oxide," and that "Takiyama [] teaches that Nishi's gate oxide may be an oxide-nitride-oxide (ONO) layer." The Final Office Action held that it would have been obvious at the time of the invention to one of ordinary skill in the art "to have an oxide-nitride-oxide layer as Nishi's oxide, as taught by Takiyama, since ONO layers are commonly known in the semiconductor art for their use as gate oxides." (Final Office Action, at pages 3-4). Appellants respectfully submit that the claims at issue are not rendered obvious over the prior art of record.

To establish a prima facie case of obviousness under 35 U.S.C. § 103, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; second, there must be a reasonable expectation of success; finally, the prior art reference (or references when combined) must teach or suggest all the claimed limitations. M.P.E.P. 2143. When applying to obviousness rejections, the references must suggest the desirability and thus the obviousness of making the combination. M.P.E.P. 2141. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 12-15 are directed to an "NROM memory cell structure" formed on a substrate, including a gate structure having an ONO composite layer and a control gate layer. The claims also define that the gate structure has a waist portion that is wider than the other two

ends thereof adjacent to the source region or the drain region, and has a hexagonal shape when viewed from the top for example (claim 12 and claim 15). The claims further recite that during a programming operation, a source-side electron injection is minimized (claim 12; specification, in paragraphs [0007] and [0008]), and second bit effect is prevented (claim 14; specification, in paragraphs [0009] and [0011]).

Nishi is directed to "a MOS semiconductor device" having a gate structure with a gate oxide for minimizing the device without reducing the operating speed of the device (Nishi, Abstract; col. 1, lines 47-50). As stated in the Final Office Action, Nishi fails to teach ONO composite layer. Takiyama, on the other hand, is also directed to "a MOS transistor" for controlling the threshold voltage without reducing the dielectric breakdown voltage of the silicon oxide and discloses merely that an ONO composite layer may be used as a gate oxide layer of a "MOS transistor" (Takiyama, col. 2, lines 56-61; col. 13, lines 40-42).

The reference teachings do not render the claims of the present invention obvious. First, it is well recognized in the semiconductor art that the gate oxide of a MOS transistor, regardless of whether it is comprised of an oxide layer or an ONO composite layer, it is invariably used for isolation, and that the functionality and the purpose of the MOS device is very different from a memory device, for example, an NROM memory device. Accordingly, the problems of the NROM memory device and approaches for resolving those problems will also be different compared to the MOS device. More particularly, as mentioned above, because Nishi is directed to size reduction of a "MOS device" and increase in operating speed thereof, and Takiyama is directed to controlling the threshold voltage also of a "MOS device". Therefore the combination of Nishi and Takiyama, in a manner suggested by the Examiner, will still result in a "MOS device". Accordingly, Applicants respectfully submit that Nishi and Takiyama cannot possibly lead one, having ordinary skill in the art at the time the invention was made, to combine the teachings of Nishi and Takiyama, in a manner suggested

by the Examiner, to make an NROM memory cell because both Nishi and Takiyam teach the "MOS device".

Second, because MOS device (regardless whether the gate oxide comprises an oxide layer or an ONO composite layer) are [not] designed for performing complex operations such as store/write/read/erase/program operations that an NROM device are designed for, and therefore the problems related to store/write/read/erase/program operations as in the case of the NROM device can not possibly occur in a MOS device. For example, NROM memory device compared to MOS device the electronic configuration of the NROM during the reading operation is different from that during the writing or the programming operation. In other words, the teachings of Nishi and Takiyama cannot possibly suggest to one, having ordinary skill in the art at the time the invention was made, that by merely replacing the [gate oxide of Nishi "MOS transistor" with the ONO composite layer of also "MOS transistor" as taught by Takiyama], could successfully make an "NROM memory device" because one skilled in the art is also presumed to be one who thinks along the line of conventional wisdom in the art and is not one who undertakes to innovate. Accordingly, the teachings of Nishi and Takiyama at best could suggest, to one having ordinary skill in the art at the time the invention was made, that the combination of Nishi and Takiyama, in a manner suggested by the Examiner, would at best produce an improved MOS device [and not an NROM device]. Accordingly, Applicants would like to point out that the question is not simply whether the prior art teaches the particular element of the invention, but whether it would suggest the desirability and reasonable level of success, and thus the obviousness, of making the combination. Neither the Nishi patent nor the Takiyama patent disclose, teach or hint the problems associated with the operation of the NROM (flash) memory cell.

Applicants would like to point out that a patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the

problem is identified. The question here is whether the prior art recognized the cause of the problem. Accordingly, because both the cited prior references, Nishi and Takiyama, are directed to a "MOS device", and therefore they could hardly recognize the cause of the problems encountering the present inventors, namely, the problems related to programming operation of an NROM memory device. Accordingly, Nishi and Takiyama cannot possibly suggest one skilled in the art at the time the invention was made to combine the teachings of Nishi and Takiyama, in a manner suggested by the Examiner, to achieve the NROM memory of the claimed invention. In other words, Nishi and Takiyama, neither alone or in combination can possibly render the structure of the NROM memory device of claimed invention.

Applicants have discovered that in a conventional NROM memory cell, the size of the source terminal and the drain terminal are roughly same or the drain terminal is bigger than the source terminal, and therefore, for example, during the programming step, this often leads to source-side electron injection causing problems such as second bit effect adversely affecting the performance of the NROM memory cell. Accordingly, discovering the cause of the source-side electron injection in an NROM memory cell, Applicants proposed remedy this problem by making the source terminal larger than the drain terminal to reduce the source-side electron injection. Accordingly, the present inventors proposed a structure of an NROM memory cell, as claimed in Claims 12-15, comprising a gate structure having a waist portion wider than the other two ends adjacent the source region and the drain region, [so that a portion of the gate structure close to the source region and the source region sever as an equivalent source region which is substantially larger than the drain terminal] so that the source-side electron injection can be minimized or reduced.

In other words, the problems confronted by the inventor must be considered in determining whether it would have been obvious to combine references in order to solve that

problem. Because both Nishi and Takiyama are substantially directed to MOS transistor and fails to even mention the problems associated with the operation of the NROM (flash) memory cell, and therefore Nishi and Takiyama cannot possibly suggest to one having ordinary skill in the art at the time the invention was made that a combination of Nishi and Takiyama in a manner suggested by the Examiner could resolve the source-side electron injection problem of the NROM memory cell. Accordingly, Applicants respectfully submit that the prior arts of record cannot possibly render each and every features of claim 12 obvious in this regard.

Applicants respectfully submit that in determining the relevant art of the claims in question one looks to the nature of the problem confronting the present inventors. Accordingly, because both Nishi and Takiyama substantially teach a MOS device, which are absolutely irrelevant to the problems of programming operation of the NROM device confronting the present inventors, and therefore the cited prior art references Nishi and Takiyama are considered as non-analogous art and therefore are not valid prior arts for this application.

Accordingly, Applicants respectfully submit that Nishi and Takiyama fail to teach, disclose, suggest or hint each and every features of the claimed invention as claimed in claims 12-15, and therefore claims 12-15 should be allowed.

Therefore, when the references as well as the claimed invention are considered as a whole, one of ordinary skill in the art would not have been suggested or motivated to combine the teachings of Nishi and Takiyama to make an NROM memory device, and, even if such a combination were made, the combination of the reference teachings [would have resulted in a MOS transistor rather than the claimed NROM memory device] of the present invention.

Accordingly, Appellants assert that claims 12-15 were not rendered obvious over the prior art of record and thus were improperly rejected under 35 U.S.C. 103(a).

IX. CONCLUSION

As noted, none of the cited art, either alone or in combination, can be said to anticipate and/or render obvious the appealed claims. Accordingly, Applicants believe claims 12-15 patentably define over the Cited Two References.

Accordingly, Applicant believes that the rejections under 35 U.S.C. § 103 are in error, and respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejections of the claims on appeal.

Respectfully Submitted,

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APPENDIX A - CLAIMS ON APPEAL

Claims 1-11 (previously canceled).

Claim 12. (previously amended) An NROM memory cell structure formed on a substrate, the cell structure comprising:

one source and one drain regions formed inside the substrate;

one gate structure formed on the substrate between the source region and the drain region, the gate structure including an oxide-nitride-oxide layer and a control gate layer sequentially stacked on the substrate, wherein said gate structure has a waist portion wider than two ends thereof respectively adjacent to the source region and the drain region and wherein a source-side electron injection is minimized when a programming action is proceeded.

Claim 13. (previously added) The NROM memory cell structure of claim 12, wherein the waist portion is roughly at a symmetrical line that runs across the central region of the gate structure between the source and the drain regions.

Claim 14. (previously added) The NROM memory cell structure of claim 12, wherein in a programming operation, a portion of the gate structure close to the source region serves as an equivalent source region such that an overall size of the equivalent source region is greater than the drain region so as to prevent a second bit effect.